Low-Density Parity-Check code for 5G-New Radio

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Document revision record

<table>
<thead>
<tr>
<th>Rev.:</th>
<th>Date:</th>
<th>Initiator:</th>
<th>Changes:</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>181002</td>
<td>TGN</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
LDPC for 5G-NR

1. Introduction

5G wireless technology is an essential technology to be launched to meet the rising demands of more connected devices, higher data speeds, rapid response times and high quality of service (QoS). To meet these requirements cost-effectively, an entirely new network architecture must be deployed. Essential to the network architecture will be a Centralized Radio Access Network (C-RAN) where Baseband Processing Units (BBUs) are separated from Remote Radio Heads (antennas - RRHs) and physically or virtually centralized in order to increase efficiency and cost-effectiveness.

To bring down bandwidth requirements between the BBU’s and the RRH’s several standards are proposing splitting the radio protocol stack, so that parts of the L1/PHY processing is taking place at the RRH side. To facilitate this new radio L1/PHY processing blocks are required for the radio systems. One of these blocks is a Low-Density Parity-Check (LPDC) encoder and decoder that can support channel coding for new 5G New Radio (NR) waveforms.

The placement of the LPDC channel coding for 5G-NR in the radio protocol is shown for Downlink and Uplink in Figure 1-1 and Figure 1-2, respectively.

This project aims to design a LDPC encoder and decoder for a radio PHY solution placed in a remote radio head.

2. Content/Goals

The project objectives are:

1. Assess and evaluate LDPC codes with a focus on decoding algorithms
LDPC for 5G-NR

2. Design an IP in VHDL/Verilog that implements a LDPC encoder and decoder using selected algorithms
3. Verify and measure the performance of the implementation in simulation
4. Being able to follow a general engineering design process with reference to the Comcores development process.

3. Project Tasks
The specific tasks to be conducted in the project are:

- Study LDPC codes with a focus on decoding algorithms
- Select decoding algorithm most suitable for hardware implementation
- Write requirement specification for a design that implements selected algorithm
- Write design specification and code RTL for the design
- Develop a testbench for testing the performance of the implementation
- Test implementation
- Document the work in a report

4. Prerequisites
The following prerequisites applies for this project:

- Experience with HDL programming (in VHDL or Verilog)
- Knowledge within the field of channel coding
  Some know-how on wireless communication systems and radio protocols (not essential)