



COMCORES

IQ Compression for 5G fronthaul

Master Thesis Proposal for Spring 2019

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1. Introduction

5G wireless technology is an essential technology to be launched to meet the rising demands of more connected devices, higher data speeds, rapid response times and high quality of service (QoS). To meet these requirements cost-effectively, an entirely new network architecture must be deployed. Essential to the network architecture will be a Centralized Radio Access Network (C-RAN) where Baseband Processing Units (BBUs) are separated from Remote Radio Heads (antennas - RRHs) and physically or virtually centralized in order to increase efficiency and cost-effectiveness.

To bring down bandwidth requirements between the BBU's and the RRH's several standards are proposing splitting the radio protocol stack, so that parts of the L1/PHY processing is taking place at the RRH side. In addition to splitting the radio protocol certain standards are also applying different compression schemes to further reduce the bandwidth.

Figure 1-1 shows how the PHY-layer of the radio protocol have been split for xRAN. Here LLS CU (Low Layer Split Centralized Unit) refers to the BBU and RU (Radio Unit) to the RRH.

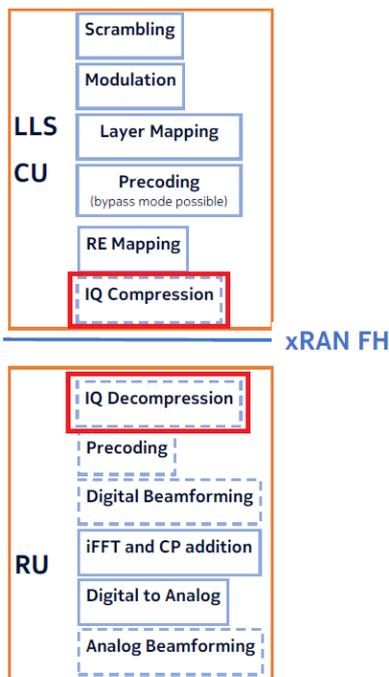


Figure 1-1: Split of radio protocol processing for xRAN

This project aims to assess the performance and trade-offs between various IQ compression methods as specified by xRAN in their "xRAN Control, User and Synchronization plane specification v2.0" and to design a solution meeting xRAN requirements.

2. Content/Goals

The project objectives are:

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1. Assess the performance and trade-offs between two (or more) of the listed IQ compression methods for xRAN.
2. Define requirements for an IP that implements one or more selected IQ compression methods based on performance assessment and general system inputs from Comcores engineers.
3. Design and verify an IP in VHDL/Verilog that implements one or more selected IQ compression methods according to the requirements.
4. Being able to follow a general engineering design process with reference to the Comcores development process.

3. Project Tasks

The specific tasks in the project are:

- Study the xRAN v2.0 standard with a focus on annex A
- Assess and evaluate performance of at least two methods using e.g. Matlab
- Write requirement specification for a block that implements a selected compression method
- Write design specification and code RTL for the block
- Test implementation both block-by-block and full top-level testing
- Document the work in a report

4. Prerequisites

The following prerequisites applies for this project:

- Experience with HDL programming (in VHDL or Verilog)
- Knowledge within the field of data compression
- Some know-how on wireless communication systems and radio protocols (not essential)

Formalities:

ECTS points: 30

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